

MULTIMEDIA



UNIVERSITY

STUDENT ID NO

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MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2019/20

EEE1016 ELECTRONICS I

(All Section / Groups)

28 FEBUARY 2020
9:00 a.m. – 11:00 a.m.
(2 Hours)

INSTRUCTIONS TO STUDENT

1. This Question paper consists of 7 pages including cover page and **List of Equations** with 4 Questions only.
2. Attempt **ALL** questions. All questions carry equal marks and the distribution of the marks for each question is given.
3. Please print all your answers in the Answer Booklet provided.

Question 1

- (a) With the use of an energy band diagram to illustrate the movement of electrons and holes, explain the electron-hole pair generation and recombination process in an intrinsic silicon (Si) crystal at room temperature. [6 marks]
- (b) A sample of Si has an intrinsic carrier concentration of 1.5×10^{10} atoms/cm³ at a temperature of $T = 300^\circ\text{K}$. The electron and hole mobilities of the Si material are $\mu_n = 1500$ cm²/V-s and $\mu_p = 500$ cm²/V-s, respectively. Donor and acceptor impurities are added into the pure Si material with concentrations of 1.25×10^{12} atoms/cm³ and 8×10^{11} atoms/cm³, respectively.
- (i) Determine the electron and hole concentrations of the extrinsic Si material at $T = 300^\circ\text{K}$. [7 marks]
- (ii) Calculate the drift current density of the extrinsic Si for $E = 32$ V/cm. [3 marks]
- (c) Draw the voltage-versus-current (V-I) characteristic curve of a practical Si type p-n junction diode. In the sketch, you must clearly indicate the cut-in voltage V_γ , the breakdown voltage V_{BR} , and the reverse saturation current I_0 of the diode. [3 marks]
- (d) For the diode circuit depicted in Figure Q1(d), a constant drop model with a cut-in voltage of $V_\gamma = 0.7$ V is assumed for the pn junction diode. Determine the following:
- (i) The diode forward current, I_f . [2 marks]
- (ii) The power dissipated by the diode, P_D . [2 marks]
- (iii) The minimum value of R , if the diode has a maximum rated current of 800 mA. [2 marks]

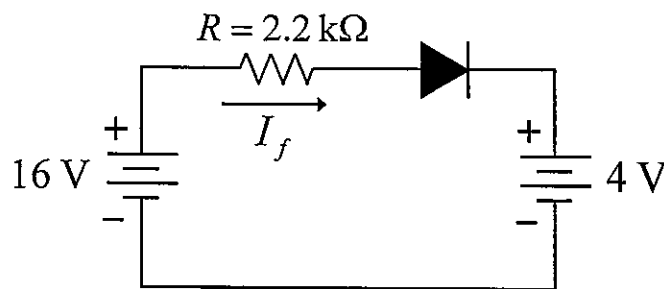


Figure Q1(d)

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Question 2

- (a) Figure Q2(a) illustrates a single-phase half-wave rectifier circuit, which is connected to a $120\text{V}_{\text{rms}}/60\text{Hz}$ AC power source via a step-down transformer with turns ratio of 10:1. Given that the load resistance $R_L = 1\text{ k}\Omega$. Assume the diode has cut-in voltage $V_\gamma = 0.7\text{ V}$, and the forward diode resistance R_f is negligible.
- Determine the average output voltage $V_{o(av)}$, and average load current $I_{o(av)}$. [3 marks]
 - Calculate the rms output voltage $V_{o(rms)}$, and rms load current $I_{o(rms)}$. [3 marks]
 - Find the ripple factor of the output voltage, γ . [2 marks]
 - Compute the average power through the load R_L , P_{dc} . [2 marks]
 - Determine the rectification efficiency, η . [3 marks]
 - Sketch the output waveform V_o with respect to the transformer secondary voltage V_s for $0 \leq \omega t \leq 4\pi$, clearly indicating the values of the respective amplitudes. [3 marks]

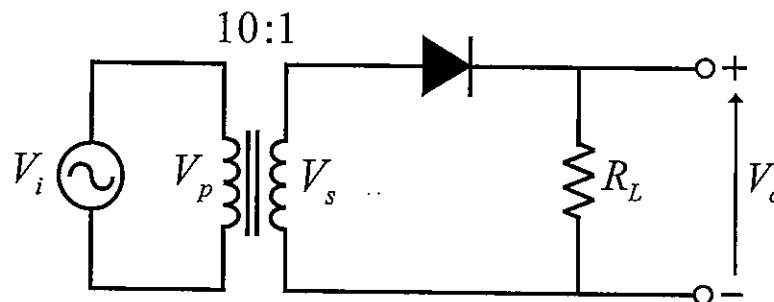


Figure Q2(a)

- (b) You are required to design limiter circuits by using Silicon (Si) and Germanium (Ge) diodes and $100\text{ }\Omega$ resistors only. Assume all Si diodes have cut-in voltage of 0.7 V and all Ge diodes have cut-in voltage of 0.3 V . The requirements of the limiter circuits are as follows:
- Clip at $+1.4\text{ V}$ and above, and -1.0 V and below. [3 marks]
 - Clip at $\pm 1.3\text{ V}$. [3 marks]

Continued ...

- (c) Figure Q2(c) shows a clamping circuit with an input voltage $V_i = 20\sin\omega t$ V. Given that the diode has a cut-in voltage of 0.7 V, and no charge is stored in the capacitor at $t < 0$. Sketch the output waveform V_o with respect to V_i , for $0 \leq \omega t \leq 6\pi$.

[3 marks]

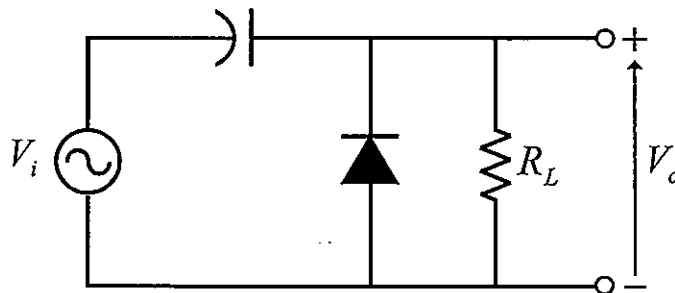


Figure Q2(c)

Question 3

- (a) In bipolar junction transistor analysis.
- Explain briefly what is Load-line, [2 marks]
 - Define what is Q-Point [2 marks]
 - Describe the procedures to draw the Q-Point, on a typical output characteristic of a common-emitter transistor circuit. [3 marks]
- (b) The Fixed bias circuit is shown in Figure Q3 (a). Given: $V_{CC}=15$ V, $R_B= 50$ k Ω , R_C 2.2k Ω , $\beta=100$. Calculate the following:
- Quiescent Input Current (I_{BQ}) [4 marks]
 - Quiescent Collector Current (I_{CQ}) [2 marks]
 - Output Voltage (V_{CEQ}) [4 marks]

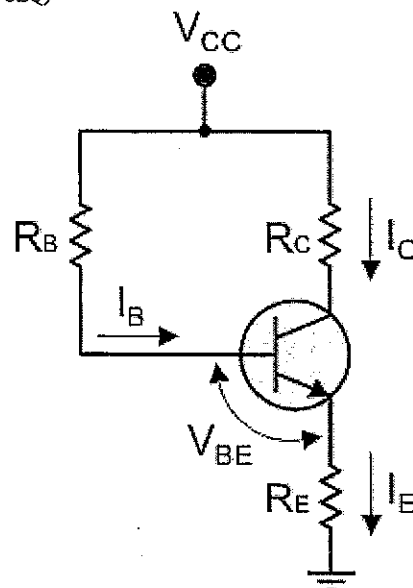


Figure Q3 (b)

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- (c) Calculate the stability factor $S(V_{BE})$ and change in I_c from 25°C to 100°C for the transistor, shown in table Q3(c) and defined by the following bias arrangement.

$T (^{\circ}\text{C})$	$I_{CO} (\text{nA})$	β	$V_{BE} (\text{V})$
-65	0.2×10^{-3}	20	0.85
25	0.1	50	0.65
100	20	80	0.48
175	3.3×10^3	120	0.3

Table Q3 (c)

- (i) Fixed bias with $R_B = 250\text{k}\Omega$ and $\beta = 100$ [4 marks]
- (ii) Emitter bias with $R_B = 240\text{k}$, $R_E = 1\text{k}$ and $\beta = 100$ [4 marks]

Question 4

- (a) Describe what it means by a “Single port circuit” and “Two port circuit” linear electric circuit. Illustrate an example of single port circuit and two port circuit. [4 marks]
- (b) The BJT common-Emitter (CE) amplifier is shown in Figure Q4 (b). Given: $V_{CC} = 18\text{V}$, $V_{BE} = 0.7\text{V}$, early voltage (V_A) = 50V , $R_1 = 47\text{k}\Omega$, $R_2 = 8\text{k}\Omega$, $R_C = 4.7\text{k}\Omega$, $R_E = 2\text{k}\Omega$, $R_S = 500\Omega$, $R_L = 1\text{k}\Omega$ and $\beta = 100$.
- (i) r_e model. [4 marks]
- (ii) r_π model. [4 marks]

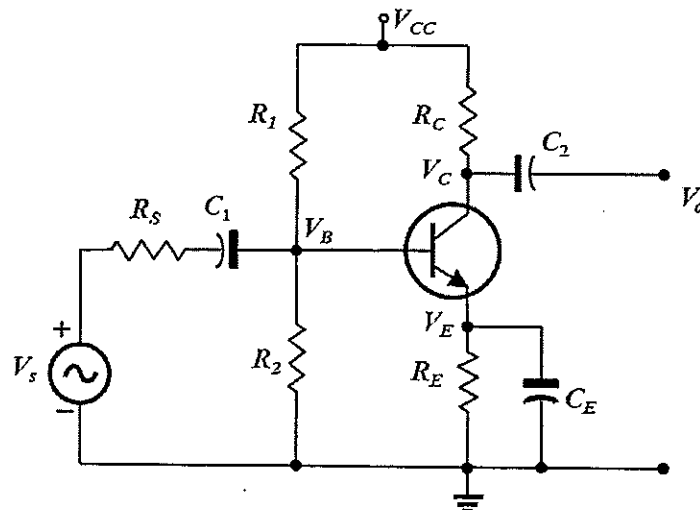


Figure Q4 (b)

Continued ...

- (c) The Bipolar Junction Transistor (BJT) Circuit is shown in Figure Q4(c) Given: $\beta = 120$, $R_S = 500\Omega$, $R_1 = 60k\Omega$, $R_2 = 10k\Omega$, $R_C = 3.2k\Omega$, $R_E = 1k\Omega$, $R_L = 1k\Omega$, $C_{in} = C_E = C_C = 10\mu F$, $V_{CC} = 15V$.

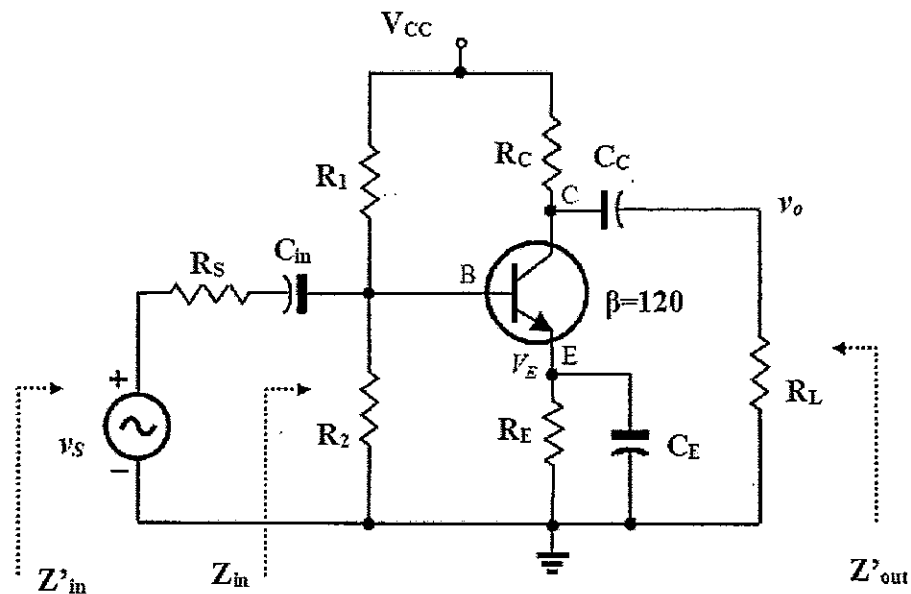


Figure Q4 (c)

- (i) Determine whether or not approximation method can be used to determine the DC voltage V_B and hence calculate V_E [5 marks]
- (ii) Determine the emitter current I_E and calculate the internal emitter resistance r_e of the BJT. [2 marks]
- (iii) Draw the r_e model of the amplifier circuit and show all the known values of its components, given that the output resistance, $r_o = \infty$. [2 marks]
- (iv) Calculate the input impedance Z_{in} and the effective input impedance Z'_{in} seen from the signal generator. [4 marks]

End of Paper

Appendix

1. Charge of electron, $q = 1.6 \times 10^{-19}$ coulomb
2. Mass of electron, $m = 9.11 \times 10^{-31}$ kg
3. Holes and electrons in pure semiconductor, $p = n = n_i$
4. Law of Mass-action, $np = n_i^2$
5. $n - p = N_D - N_A$
6. $J_{drift} = q(n\mu_n + p\mu_p)E$
7. $V_{o(av)} = V_{dc} = \frac{V_m}{\pi}$
8. $I_{o(av)} = I_{dc} = \frac{I_m}{\pi} = \frac{V_m}{\pi R_L}$
9. $\gamma = \sqrt{\left(\frac{V_{o(rms)}}{V_{o(av)}}\right)^2 - 1}$
10. $P_{dc} = I_{o(av)}^2 R_L$
11. $P_{rms} = I_{o(rms)}^2 R_L$
12. $V_{CC} = I_B R_B + V_{BE}$
13. $V_{CC} - V_{BE} = I_B R_B$
14. $V_{CC} = I_C R_C + V_{CEQ}$
15. $V_{CEQ} = V_{CC} - I_C R_C$
16. $\beta R_E > 10 R_2$
17. $S(V_{BE}) = \left(\frac{-\beta}{R_B + (\beta + 1)R_E} \right)$
18. $\Delta I_C = S(V_{BE}) \cdot \Delta V_{BE}$
19. $V_B = \frac{V_{CC} R_1}{R_1 + R_2}$

